

REMARKS

The application has been amended to place it in condition for allowance at the time of the next Official Action.

Claims 1-8 were previously pending in the application. New claims 24-28 are added. Therefore, claims 1-8 and 24-28 are presented for consideration.

Claims 1-8 are rejected as anticipated by applicants' disclosed prior art. This rejection is respectfully traversed.

Claim 1 provides that the first wiring-arrangement section has a first test section is formed and subjected to a provisional yield-rate test. Claim 1 also provides that the second wiring arrangement section is formed when the wafer passes the provisional yield-rate test. Accordingly, a first wiring section is formed, a yield test is performed, then a second wiring section is formed.

As seen in prior art Fig. 16 of the present application, and as disclosed on page 37, lines 21-26 of the present application, the conventional semi-finished semiconductor device includes basic wiring arrangement section 16' and custom-purpose wiring arrangement section 48'. These two wiring sections 16' and 48' are the only wiring sections and are both formed before the yield rate test is performed.

Accordingly, the disclosed prior art teaches forming first and second wiring sections before a yield rate test, not

forming a first wiring section then performing a yield-rate test and then forming a second wiring section, as recited.

As the reference does not disclose that which is recited, the anticipation rejection is not viable. Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 2-8 depend from claim 1 and further define the invention and are also believed patentable over the cited prior art.

New claims 24-28 include the steps of forming a first wiring section then performing a yield-rate test and then forming a second wiring section. New claims 24-28 are also believed patentable over the cited prior art at least for the reasons set forth above with respect to claims 1-8. Support for new claims 24-28 can be found in Figures 4 and 5, for example.

New claim 29 includes the steps of forming a first multilayer wiring arrangement section on a chip area as a semi-finished semiconductor device. Claim 29 further provides performing a provisional yield-rate test to determine whether the first wiring-arrangement section is acceptable or unacceptable and then forming a second multilayer wiring arrangement section on the first multilayer wiring arrangement section as a finished semiconductor device.

Disclosed prior art Figures 16 and 17 and the accompanying passage on page 35, lines 8-28, disclose that the semi-finished semiconductor device includes multilayer wiring arrangement 16' and multilayer wiring arrangement 48'. As seen in prior art Fig. 16, layers 16' and 48' are the only multilayered wiring arrangements.

As disclosed on page 36, lines 21-25, a yield-rate test is performed on the semi-finished semiconductor device that includes both layers 16' and 48'. Thereafter, the uppermost circuit pattern is rearranged and customized in accordance with a customer's request, as disclosed on page 36, lines 27-31. Accordingly, the conventional method forms both the first and second wiring arrangements as seen in Figure 16 and then a yield-rate test is performed. In contrast, claim 29 recites that the first wiring layer is formed then a yield-rate test is performed and then the second wiring layer is performed.

Accordingly, new claim 29 is believed to avoid rejection under §102 and is believed patentable over the art of record.

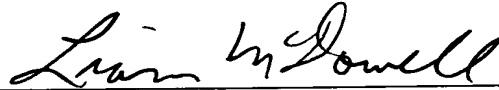
In view of the present amendment and the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional
fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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